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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/576,348	04/18/2006	Kenji Kawakami	1163-0565PUS1	9490

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EXAMINER	
STEVENS, GERALD D	

ART UNIT	PAPER NUMBER
2817	

NOTIFICATION DATE	DELIVERY MODE
12/11/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/576,348	KAWAKAMI ET AL.	
	Examiner	Art Unit	
	GERALD STEVENS	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *2,4,6,9,11 and 13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,8,10,12 and 15-28* is/are rejected.

7)☒ Claim(s) *7 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the communications filed on 30 July 2008.

2. Claims 1,3,5,7,8,10,12,14, & 15-28 are pending with none of the claims being amended and claims 2,4,6,9,11, & 13 being cancelled.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 5, 8, 10, 12, 15-20, & 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al (cited by applicant, US 7164902 used for interpretation) in view of Belfatto (both of record).

Regarding claims 1, 5, 8, 12, 15-20, & 23-26, Yamada (e.g. fig. 1) exemplarily teaches having a filter-integrated even harmonic mixer comprising: two transmission line sections (22 & 27, i.e. a branching means) that are arranged to receive an intermediate frequency signal (f_{IF}, i.e. a pulsed signal) from an f_{IF} terminal (31, i.e. pulse applying terminal), receive a local oscillation signal (f_{LO}) from a local oscillation signal terminal (33, i.e. local oscillation wave input terminal), and for outputting a high-frequency signal (i.e. a pulsed signal) having a frequency of $f_{IF} + 2x\ f_{LO}$ (i.e. frequency even times local oscillation) to a high-frequency signal terminal (34, i.e. pulse output terminal). The high-frequency signal is delivered to the high-frequency signal terminal (34) via an anti-parallel diode pair (25, i.e. mixing means, i.e. **claims 15,16**), which

receives the local oscillation signal (f_{LO}) and the intermediate frequency signal (f_{IF}) and mixes them to produce the high-frequency signal. Inherently, the diodes within the anti-parallel diode pair (25) each produce a second harmonic that is in opposite phase with respect to the other since the diodes are connected in an anti-parallel configuration (i.e. **claims 19,20**). To deliver only the high-frequency signal (i.e. frequency even times local oscillation) and to block all other signal components from the output of the anti-parallel diode pair (25, i.e. mixing means) is a bandpass filter (23), which passes the filtered signal to the high-frequency signal terminal (34, i.e. **claims 17,18**). Connected at a connection point between the local oscillation signal terminal (33) and the anti-parallel diode pair (25) is a one-quarter wavelength short stub (26, i.e. **claims 23 & 24**), see col. 5 lines 47-48,

but fails to teach having a voltage dividing means for dividing a voltage applied to said mixing means.

Belfatto (e.g. sole figure) exemplarily teaches having a pulse modulator comprising: bias resistors (36,38,40, i.e. voltage dividing means) that are located between a modulation input pulse source (34) and a mixer (28).

It would have been obvious to one having ordinary skill in the art at the time of the invention to have added the bias resistor network such as taught by Belfatto to the f_{IF} terminal of the filter-integrated even harmonic mixer circuit such as taught by Yamada because the bias resistor network of Belfatto provides the benefit of setting a proper signal level for the circuit to which it is being applied (col. 2 lines 40-42).

Therefore, as an obvious consequence of the above combination, the bias resistors (Belfatto: sole fig. resistors 36,38,40) are located after the f_{IF} terminal (Yamada: fig. 1 terminal 31, (i.e. **claims 25,26**). This resultant configuration results in the resistor (Belfatto: sole fig. resistor 36) is disposed between the f_{IF} terminal (Yamada: fig. 1 terminal 31, i.e. pulse applying terminal) and ground (i.e. **claims 5,12**).

Regarding claims 3 & 10, the above combination teaches all of the elements as discussed above in claims 1 & 8, respectively, but fails to teach having the resistor comprising the voltage dividing means being a variable resistor.

Belfatto (e.g. sole figure) exemplarily teaches having a pulse modulator comprising: a potentiometer (52) connected in series with a fixed resistor (50). Together the potentiometer (52) and fixed resistor (50) are used to control the amplitude of an output signal (col. 2 lines 66-68).

It would have been obvious to one having ordinary skill in the art at the time of the invention to have replaced the bias resistor network such as taught by the above combination with the series connected fixed resistor and potentiometer such as taught by Belfatto because it is obvious to have used an art equivalent attenuation circuit such as taught by Belfatto in the place of another equivalent attenuation circuit such as taught by the above combination.

3. Claims 21 & 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Belfatto as applied to claims 1 & 8, respectively, above, and further in view of Dobrovolny (all of record).

Regarding claims 21 & 22, the above combination teaches all of the elements as discussed above in claims 1 & 8, respectively, but fail to teach having a voltage dividing means comprising a parallel circuit comprising a resistor and a capacitor, which is disposed between the mixing means and a ground or between the branching means and the mixing means.

Belfatto (e.g. sole figure) exemplarily teaches having a pulse modulator comprising: an attenuator (54) located at the output of a mixer (28).

It would have been obvious to one having ordinary skill in the art at the time of the invention to have added the attenuator such as taught by Belfatto to the output of the anti-parallel diode pair such as taught by the above combination because the attenuator of Belfatto provides the benefit of adjusting the level of the mixer output signal to a desired level (col. 3 lines 3-5).

Therefore, as an obvious consequence of the above combination, the attenuator (Belfatto: sole fig. attenuator 54) is located between the anti-parallel diode pair (Yamada: fig. 1 element 25) and the two transmission line sections (Yamada: fig. 1 elements 22 & 27).

Dobrovolny (e.g. fig. 2) exemplarily teaches having a single balanced down converter mixer comprising: a biasing network composed of a parallel connected capacitor (24) and resistor (22).

It would have been obvious to one having ordinary skill in the art at the time of the invention to have replaced the attenuator located at the output of the anti-parallel diode pair such as taught by the above combination with the biasing network such as taught by Dobrovolny because it is obvious to have used an art equivalent attenuating circuit such as taught by Dobrovolny in the place of another equivalent attenuating circuit such as taught by the above combination.

4. Claims 27 & 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Belfatto as applied to claims 25 & 26, respectively, above, and further in view of Wheatley (all of record).

Regarding claims 27 & 28, the above combination teaches all of the elements as discussed above in 25 & 26, respectively, but fails to teach the voltage dividing means further comprising a serial circuit comprising said resistor and a diode, wherein said circuit is disposed between the pulse applying terminal and the branching means. Wheatley (e.g. fig. 1) exemplarily teaches having a balanced mixer comprising: an attenuator circuit composed of a series connected circuit containing a resistor (16), a diode (20), and a potentiometer (20).

It would have been obvious to one having ordinary skill in the art at the time of the invention to have replaced the bias resistors such as taught by the above combination with the attenuator circuit such as taught by Wheatley because it is obvious to have used an art equivalent attenuation circuit such as taught by Wheatley in the place of another equivalent attenuation circuit such as taught by the above combination.

Allowable Subject Matter

5. Claims 7 & 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments with respect to claims 1 & 8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GERALD STEVENS whose telephone number is (571)270-5076. The examiner can normally be reached on Mon-Fri 7:30am - 5:00pm EST alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GDS

/Robert Pascal/
Supervisory Patent Examiner, Art Unit 2817